

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Li Attorney Docket: 2003 P 54557 US  
Filed: Herewith Examiner: TBD  
Serial No.: TBD Art Unit: TBD  
For: Transistor with Doped Gate Dielectric

Mail Stop: Patent Application  
Commissioner for Patents  
P. O. Box 1450  
Alexandria, VA 22313-1450

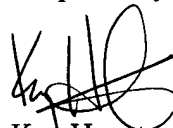
**INFORMATION DISCLOSURE STATEMENT**

Dear Sir:

The Applicant wishes to bring to the attention of the Patent and Trademark Office the information noted on the enclosed form PTO/SB/08A that may be considered material to the examination of the above-identified application.

No fee is due at this time, as this Information Disclosure Statement is being filed concurrently with the patent application.

Respectfully submitted,



Kay Houston  
Attorney for Applicant  
Reg. No. 38,495

February 3, 2004

Date

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  <i>(use as many sheets as necessary)</i>			Application Number	TBD
			Filing Date	HEREWITH
			First Named Inventor	Li
			Art Unit	TBD
			Examiner Name	TBD
Sheet	1	of	Attorney Docket Number	2003 P 54557 US

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code <sup>2</sup> (if known)			
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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
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OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
	1	INUMIYA, S., <i>et al.</i> , "Fabrication of HfSiON Gate Dielectrics by Plasma Oxidation and Nitridation, Optimized for 65nm node Low Power CMOS Applications," 2003 Symposium on VLSI Technology Digest of Technical Papers, pp. 18-19, Document No. 4-89114-035-6/03.	
	2	WOLF, S., "Silicon Processing for the VLSI Era: Diffusion in Silicon" pp. 336-339.	

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\*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup>Applicant's unique citation designation number (optional). <sup>2</sup>See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup>Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup>For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup>Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup>Applicant is to place a check mark here if English language Translation is attached.

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